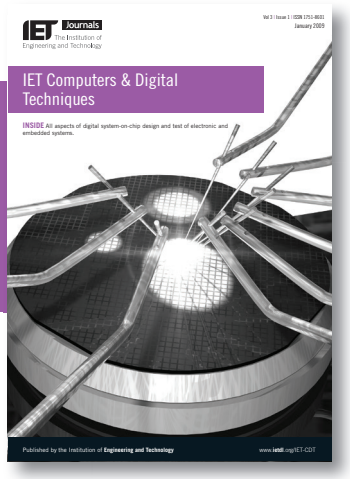
IET Journals
The Institution of Engineering and Technology



IET Computers & Digital Techniques
Call for Papers

SPECIAL ISSUE ON:
Emerging On-Chip Networks and Architectures

By entering into the ultra deep sub-micron (UDSM) era, the role played by the on-chip communication system is getting more and more relevance. In fact, as technology shrinks, gates become faster and more power efficient whereas wires become slower and more power hungry. Thus, the on-chip communication system represents one of the most important elements which determine the overall performance, cost, reliability, and energy consumption of a modern multi-processor system-on-chip (MPSoC).

The goal of the Special Issue is to provide a forum for researchers to present innovative ideas and solutions related to design and implementation of multi-core systems on chip. This Special Issue will focus on issues related to design, analysis and testing of on-chip and on-system networks. The topics of specific interest for the workshop include, but are not limited to:

- Topologies selection and synthesis for NoCs and MPSoCs
- Routing algorithms and router micro-architectures
- QoS in on-chip communication
- Mapping of cores to NoC slots
- Power and energy issues
- Fault tolerance and reliability issues
- Memory architectures for NoC
- Dynamic on-chip network reconfiguration
- Modeling and evaluation of on-chip networks
- On-chip interconnection network simulators and emulators
- Analytical analysis methods for NoC performance and other properties
- Verification, debug and test of NoC
- 3D NoC architectures
- Emerging technologies and new design paradigms
- Industrial case studies of SoC designs using the NoC paradigm

Selected papers from the NoCArc'2012 workshop will be invited to submit an extended version of their paper. In addition, any other high quality submission that fits the topics of this Special Issue are welcome. All invited papers will be subjected to the same rigorous review process as the regular submissions to this Special Issue. Submitted articles must not have been previously published or currently submitted for publication elsewhere. For work that has been published previously in a workshop or conference, it is required that submissions to the Special Issue have at least 40% new content. Submissions that do not meet this requirement will be rejected without review.

Papers should be submitted via Manuscript Central and should adhere to standard formatting requirements. Visit **http://mc.manuscriptcentral.com/iet-cdt**

Proposed publication schedule:

Submission Deadline:
31 January 2013
Notification of Interim Decision:
31 April 2013
Revised Paper Submission:
15 June 2013
Final Decision:
30 July 2013
Final Paper:
15 August 2013

Special Issue guest editors:

Maurizio Palesi
Kore University of Enna, Italy
http://www.unikore.it/mpalesi/

Terrence Mak
Department of Computer Science and Engineering
The Chinese University of Hong Kong, China
http://www.staff.ncl.ac.uk/terrence.mak/

Masoud Daneshtalab
Department of Information Technology
University of Turku, Finland
http://users.utu.fi/masdan/